STRAINED SILICON MOSFET HAVING REDUCED LEAKAGE AND METHOD OF ITS **FORMATION**

Inventors: Qi Xiang et al. Attorney: Ronald Coslick – 039153-0668 FOLEY & LARDNER – (310) 277-2223

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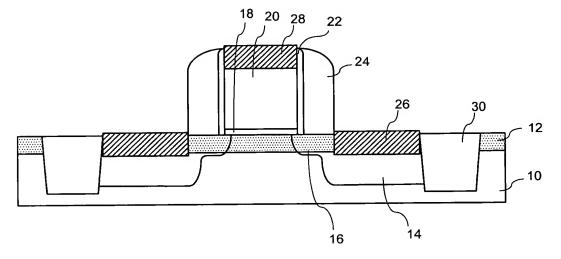


Figure 1

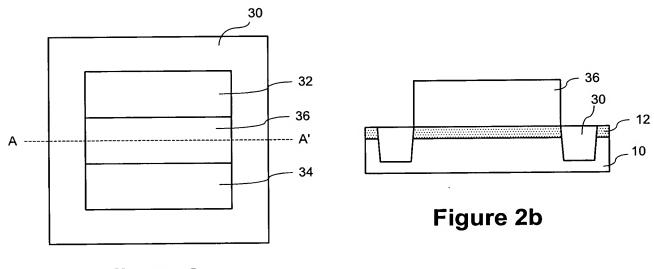
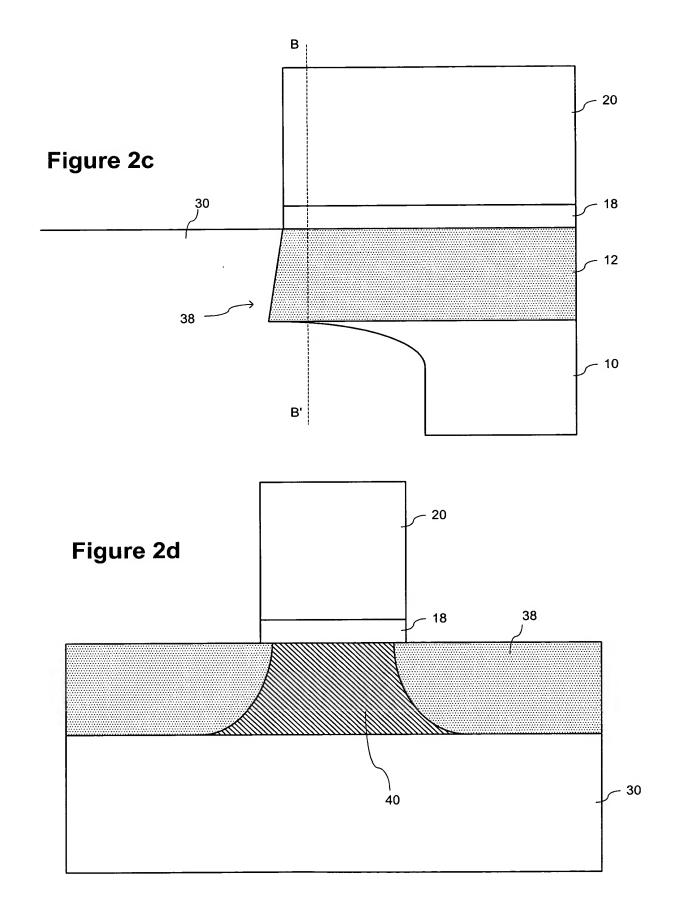


Figure 2a

STRAINED SILICON MOSFET HAVING REDUCED LEAKAGE AND METHOD OF ITS FORMATION Inventors: Qi Xiang et al. Attorney: Ronald Coslick – 039153-0668 FOLEY & LARDNER – (310) 277-2223 Sheet 2 of 7



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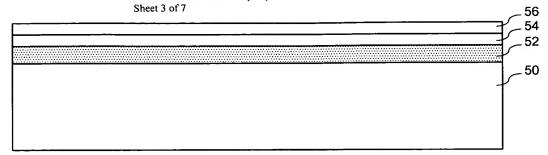


Figure 3a

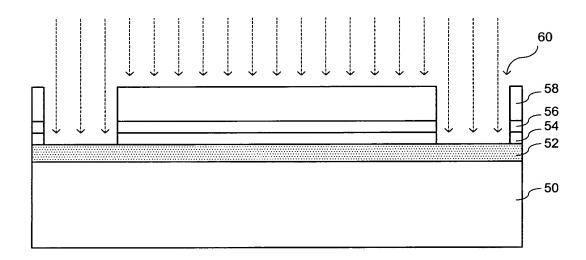


Figure 3b

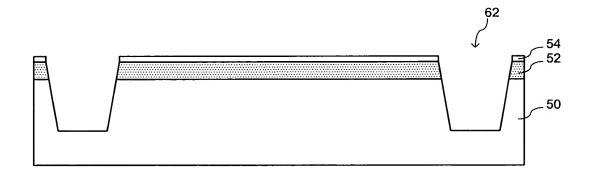


Figure 3c

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Inventors: Qi Xiang et al. Attorney: Ronald Coslick – 039153-0668 FOLEY & LARDNER – (310) 277-2223

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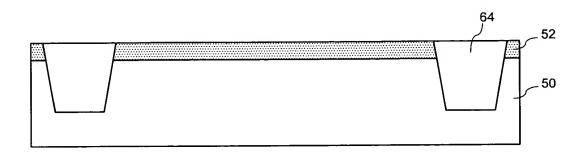
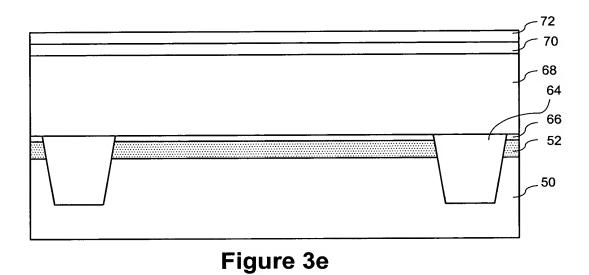


Figure 3d



76 74 52 . 50

Figure 3f

STRAINED SILICON MOSFET HAVING REDUCED LEAKAGE AND METHOD OF ITS **FORMATION**

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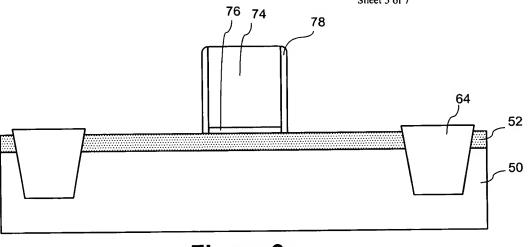
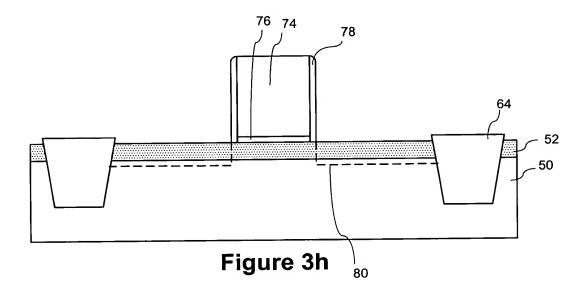
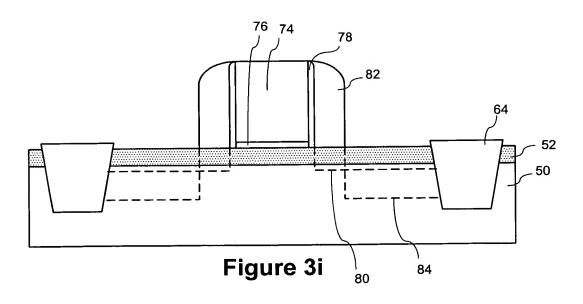


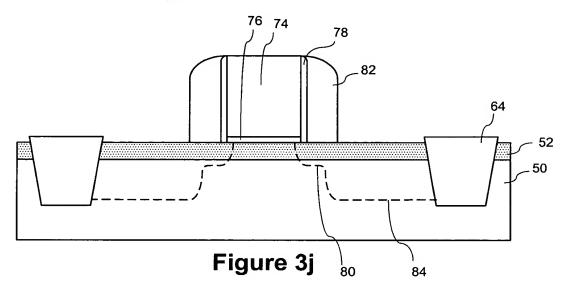
Figure 3g

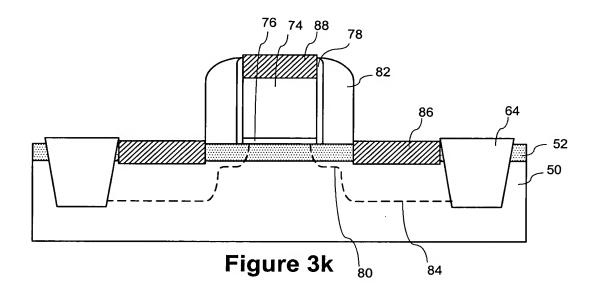




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Attorney: Ronald Coslick - 039153-0668 FOLEY & LARDNER - (310) 277-2223 Sheet 7 of 7 90 Provide a substrate including a layer of silicon germanium and a layer of strained silicon 92 Provide a mask on the strained silicon layer that defines exposed areas for shallow trench isolations 94 Perform ion implantation to damage the strained silicon in the exposed areas 96 Etch the strained silicon and silicon germanium in the exposed areas to from trenches 98 Form shallow trench isolations in the trenches 100 Form a MOSFET including the strained silicon in an active area defined by the shallow trench isolations

STRAINED SILICON MOSFET HAVING REDUCED LEAKAGE AND METHOD OF ITS

FORMATION

Inventors: Qi Xiang et al.

Figure 4